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A High Frequency Self-Reconfigurable Battery for Arbitrary Waveform Generation

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Summary

This article presents an innovative self-reconfigurable battery (SRB) architecture, which is able to generate directly at its output any waveform signals. Thanks to the specific characteristic of the proposed system, it is even possible to dispense with any AC charger. Although the individual control of each cell in the battery pack to perform an efficient active cell balancing has been already studied in the literature, the system presented in this article is the first of its kind. This article describes a real prototype of a high frequency SRB of 128 cells and demonstrates that it can be charged without any dedicated charger directly on the electrical grid, by generating a sinusoidal waveform voltage, while perfectly balancing the cells in real time.

Keywords: Battery Management System (BMS), Self-Reconfigurable Battery (SRB), multilevel converter, high efficiency conversion, active balancing.

1 Introduction

Lithium-ion batteries are widely seen as a promising solution for both power generation, as in electric vehicles, and energy storage, to cope with the variable and intermittent renewable energy. Despite providing great performance through high energy density and long service life, lithium-ion batteries require an accurate monitoring to ensure the user's safety. Indeed, high temperature, overcharge and over-discharge damage the cell and endanger the user. Therefore, all battery pack includes a Battery Management System (BMS) to stop charging and discharging the battery as soon as one cell exits its safe operating area, as described in [1].

This represents a critical limitation as unbalancing State of Health (SoH) can cause some weak cells to reach end of charge and discharge much sooner than others [2]. According to [3], 350 cycles separate the end of life of the best and worst cells of a same battery pack. For technical, economic and environmental considerations, balancing strategies [4] were developed to equalize the state of charge of cells.

Typical balancing used in most of manufactured Li-ion battery systems consists in dissipating some energy of the fully charged cells to achieve the charge of the other cells. This solution compensates only a difference in coulometric efficiency between cells and not a difference in capacity. It is always the weakest cell that limits the

capacity of the full battery pack and which ends up being the most exploited. Then the weakest cell becomes the most aging, which increases capacity differences over the time.

In order to use the full capacity of all cells of a battery pack, more advanced balancing strategies are applied such as active balancing, which use power electronic components to exchange energy from the strongest cells to the weakest ones. Other strategies use Self Reconfigurable Battery architectures (SRB) enabling to manage the average current drawn on each cell to provide the output power [5]. Some studies address the efficiency improvement of adjusting the output voltage by such battery reconfiguration compare to the use of an external DC/DC converter [6]. Others have proposed to generate a staircase shape sinusoidal waveform in order to replace the AC/DC battery charger [7] as well as the DC/AC motor inverter [8]. This is an attractive prospect as it is well known that a great amount of energy is lost in AC-DC inverters [9].

Staircase shape waveform are usually generated from multilevel converters using carrier phase shift Pulse Width Modulation (PWM) or carrier cascaded PWM [10]. Modular Multilevel Converter (MMC) with Battery Energy Storage System (MMC-BESS) have been proposed as a new three-phases topology using SRB for the traction drive [11] as well as for stationary batteries for fast charge EV charging station [12] [13]. In those studies, MMC-BESS are used in single star topology with cascaded H-Bridge, or whether in dual-star topology with only half-bridge chopper switches and twice the required number of cells. Both incorporate one to several cells in series per adjustable series level in the MMC. Due to the high number of levels, the generated three-phase AC signal offers a low total harmonic distortion (THD) on the output voltage and current. This considerably reduces the need for output power filtering and shows direct benefits on the motor efficiency [14]. Among the SRBs capable of generating sinusoidal waveforms, few offer direct on-grid recharging and all use cascaded carrier PWM control schemes. These, when embedded, are implemented on DSP and FPGA targets, and refreshed at only few KHz. Moreover, sudden fluctuations in network voltage require immediate adjustment of the output voltage, which can be difficult to achieve with such control schemes. In addition, the occurrence of cell faults requires the ability to overcome failures to avoid unexpected carrier offset under various modulation indices [15].

This paper demonstrates the feasibility of embedding cell-switching strategies in a microcontroller with the use of field buses, low voltage MOSFET as well as a single current sensor. The aim is to obtain a cost efficient SRB able, on the one hand, to charge itself directly on the power grid while reducing the requirement of passive filtering components, on the other hand to generate a perfect output waveform signal. All this while allowing the exclusion of defective cells and performing real-time cells balancing. For this purpose, this document is composed as follows: a first section introduces SRB fundamentals as well as those more specific of the proposed system. A second section describes the hardware architecture implemented. Then, a third section describes the software advanced functions. A following section presents the experimental results, such as SoC balancing, THD and efficiency of the HF SRB, through the implementation of a real demonstrator of 128 cells. Finally, a last section concludes on the performances demonstrated by the results obtained and develops the perspectives that follow.

2 SRB fundamentals

The key idea of SRB is to introduce individual control of each cell in the battery pack thanks to dedicated switches placed in series and in parallel with each cell. With such management, it becomes possible to disconnect only the weakest or damaged cells and provide the required power with the remaining ones. Moreover, bypassing switches offer the capability to adjust the number N of cells placed in serial and thus to adjust the output voltage of the battery. The generation of an AC waveform voltage from a SRB rely on the sequential superimposition of each cell voltages resulting in a staircase shape signal as shown in Fig. 1. A cell insertion increases the output voltage of one cell voltage, we name that voltage increment a “Level”, “Level 1” being the first step, and “Level n”, the n^{th} step. A level is not attached to a particular cell, any cell of the battery pack can ensure that level. As shown on Fig.1, each level performs four switching operation within a sinusoidal period. Therefore, in order to generate a 50 Hz sinusoidal waveform, the switching frequency of a level is 200 Hz. However, in order to generate an accurate waveform in its steepest part, it is necessary to respect a minimum time $TimeStep_{min}$ between two level

changes. In the case of a sine wave, the min time step must be less than or equal to the period of the fundamental harmonic of the voltage over more than six times the number of levels N_{max}.

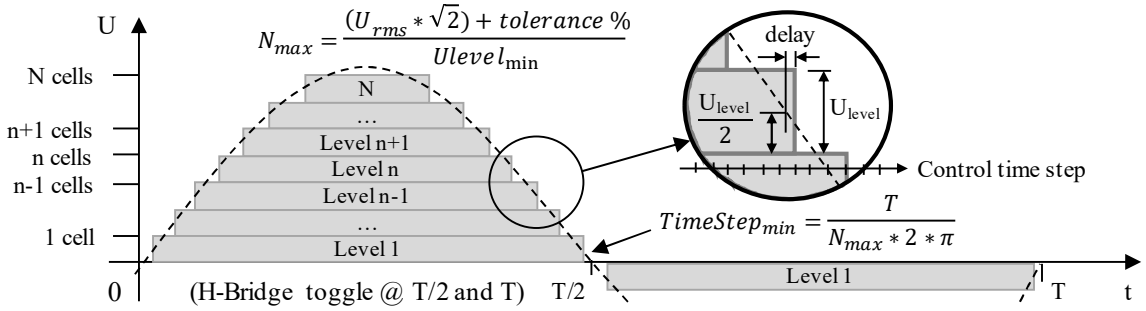
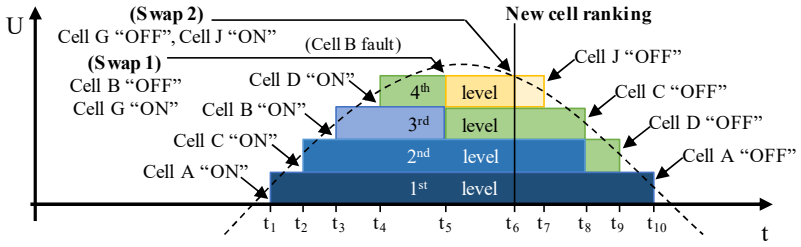


Figure 1: Staircase shape sine waveform generated by N-level SRB

When taking EU electrical network voltage as an example, which is 230 V_{RMS} +/- 10% with a frequency of 50 Hz, and using cells which the specified end of discharge threshold is 2800 mV, N_{max} reaches 128 and the related minimum time step is then about 25 µs, which corresponds to an equivalent switching frequency of 40 kHz. This frequency can be reduced if more than one level can be switched at each control time step. Note that the battery pack could include additional cells that could be used to provide the maximum voltage output in case of cell failures; therefore, the number of cells could be greater than N_{max} without affecting $TimeStep_{min}$.

Recharging an SRB directly on the electrical network consists in tracking the electrical network voltage and applying a slightly smaller voltage at the SRB output. The small voltage difference δV is applied to the internal impedance of the SRB Z_{SRB}. This induces a current exchange approximately proportional to that voltage difference which can reaches 0.5 A/V for a SRB of 128 levels of single 18650 NMC cells as Sony VTC6. Therefore, generating a waveform for charging purpose imply a tightly synchronization with the electrical network voltage waveform to avoid any excessive current exchange due to control time delay, as detailed in section 4.2. The periodic aspect of the electrical network voltage facilitates this control. However, it can present stochastic deformations, which is why a power filtering stage is usually required in existing SRBs to filter out these unpredictable disturbances.

The control strategy implemented in the proposed system is then quite different than carrier cascaded PWM in order to be embedded on microcontrollers. Here, a nearest level control (NLC) is performed. The number of serial levels to activate is then determined in real-time by rounding up to the nearest integer the real value given by a closed-loop control. The use of NLC for SRB driving have been compared with carrier cascaded PWM in [16]. It is shown that PWM control patterns tend to have a better THD when a low number of serial levels is used, while NLC induces less loss due to the reduced amount of commutations. This study has been done on a SRB of 9 levels of unit blocks having 5 cells in series, therefore the NLC THD results should be better with higher number of levels.



Cell order	X $t < t_4$	X $t_4 < t < t_6$	X $t > t_6$
1	Cell A	Cell A	Cell A
2	Cell C	Cell C	Cell D
3	Cell B	Cell D	Cell C
4	Cell D	Cell G	Cell J
5	Cell G	Cell J	Cell G
6	Cell J		

Available cells number

Figure 2: On the fly cells switch principle

Waveforms generated with our system are similar to those from carrier cascaded PWM but the management of electrical grid disturbances as well as cells faults are now possible within a half cycle of the sinusoidal voltage without signal perturbation. A control loop updates the reference waveform in real time, which allows a forthwith

management of the electrical network voltage perturbations. The First In First Out (FIFO) principle is applied to connect and disconnect the cells. The selection of the cell to be connected or disconnected is performed on the fly in a priority order provided by a balancing algorithm. The failing cells are handled forthwith without disturbing the generated waveform thanks to a cell swap operation. The cell use priority order is given by a ranking X(t), which is updated over the time from the availability of the cells and by the balancing algorithm. As illustrated in Fig. 2, the first four levels are connected from time t_1 to t_4 according to the reference signal. At time t_5, a fault occurs on cell B, which is associated with the third level. This faulty cell is disconnected and instantly removed from the list of available cells list in the ranking X(t). This ranking gives cell G as the next available cell to be connected in replacement of the faulty cell. At time t_6, the cell ranking X(t) is updated by the balancing algorithm. Cell G, now with rank five, is immediately replaced by cell J which has now rank four. Then cell J is disconnected at t_7 when only three levels are required in order to follow the theoretical waveform. At time t_8, only two levels are required and cell C is disconnected as requested by the ranking X(t). At time t_9, only one level is required and the cell D is disconnected. At time t_{10}, the zero-crossing point of the voltage is reached. The cell A is disconnected and then all cells are bypassed. The negative part of the waveform is generated thanks to inverter H-Bridges distributed on each module containing 4 cells (see Fig. 3) and cells are connected successively in the order given by the cell ranking X(t) (cell A first). The following sections show how the CEA has implemented the innovations presented above.

3 Hardware architecture

3.1 Master/Slave organization

Distributed systems have been commonly used in classical BMS implementation to address large cable bundles issues. They are based on a central unit and multiple remote units where remote units are arranged against groups of cells. SRB requires the use of switches whose number and control complexity increases with the number of cells used as well as the number of degrees of freedom it integrates (serial, parallel, serial and parallel, etc...). Some works address the complexity of a centralized control of all switches by using neural network and reinforcing learning to optimize the control strategy [17]. Others propose the use of different levels of abstraction distributed on different processing units to reduce this complexity [18]. Others even propose to distribute the control decision at different levels [19] [20].

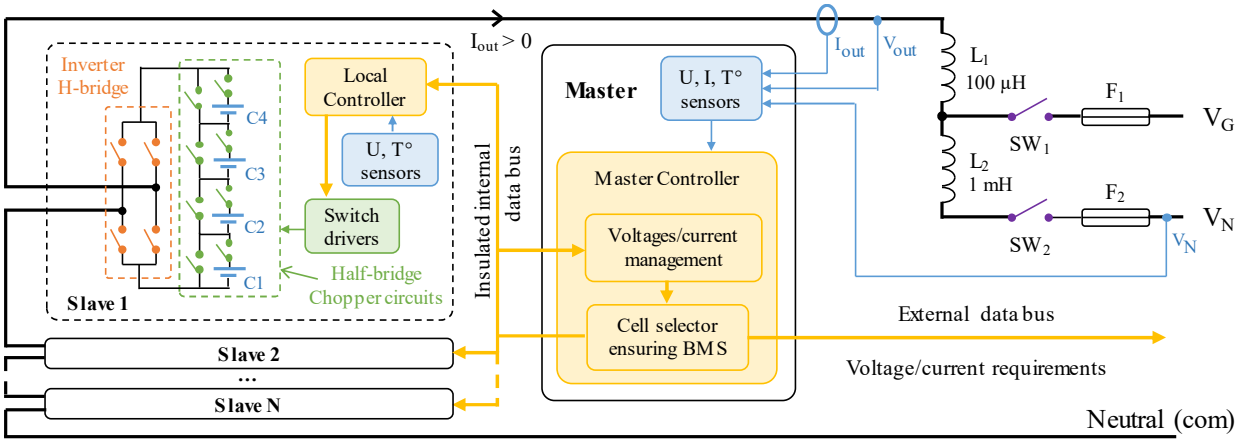


Figure 3: HF SRB hardware architecture

We propose to exploit the concept of distributing switches and their physical drivers over the battery pack while maintaining centralized control of the overall cell layout and monitoring. For this purpose, the SRB is divided into remote modules named “Slave” and a central module named “Master”. As argued in section 3.4, each Slave is composed of four serial cells connected through half-bridge chopper circuits, an H-Bridge to reverse the polarity of the module, and a local controller. Then Slaves are chained to reach the required output voltage. An

overview of the overall hardware architecture is given in Fig 3. V_{out} is the output-to-com voltage of the HF SRB, V_N is the line-to-neutral voltage into which the AC charger voltage comes in, and V_g is the generated AC voltage for the batteries discharging.

The Master module is in charge of managing all slave modules thanks to a master controller. It estimates the state of each cell and manages the safety according to data collected through the remote modules (mainly cells' voltage and temperature). The selection of the cells to be inserted in the power path is performed in the master controller while Slaves ensures switches actuation and cells parameters measurement. However, [19] advises to perform the cell selection in a distributed way, otherwise the control latency will increase significantly with the number of serial levels used in a SRB. In section 4.1 we will show how to deal with this issue and what is the impact of increasing the number of levels over the driving latency with the proposed solution. The centralized management of the SRB allows to use very low-cost local controllers. The use of a shared communication bus is required in order to reduce the number of wires in the system. These must be carefully designed to withstand disturbances related to switching, as shown in the section 3.2.

3.2 Communication buses

The splitting of the SRB into a distributed system requires the use of a reliable communication bus for safety reasons. The generation of arbitrary waveforms implies real-time constraints on the transmitted commands. The CAN bus is reliable but not suitable for transmitting commands at high frequency. The reliability of a faster real-time communication bus like USART can be enhanced by the use of a differential transmission lines as well as additional software mechanisms such as cyclic redundancy check (CRC).

Switch command messages are less critical than cells voltage and cells temperature data. Indeed, the safety of the switch control is ensured at the level of the local controller while the real time control loop performed at the master can compensate a wrong number of activated serial levels as soon as the next control time period occurs. We propose to separate real-time data from critical data by using a combination of CAN and RS485 busses. In this way, real-time data can be transmitted at higher frequency while critical data can be safely transmitted at low frequency with a lower bandwidth.

3.3 SRB control strategy

Iteratively changing the number of serially active levels allows the master controller to communicate individually and asynchronously with each local controller in order to locally modify the configuration of the cells. Thus, each local controller is only called when one of its cells is concerned by the refresh of the serial arrangement. The control frequency is limited by the master controller since the local controllers are called asynchronously at low frequency. While this sequential control has the potential to allow high command frequencies, only a few serial levels can be controlled at a time, as the length of the control message is limited by the length of the control period. A higher control frequency could be achieved by distributing the control of the slaves over several buses.

An alternative could be to transmit the required number of active levels in series to all the local controllers in a single message sent over the real-time communication bus. The rank of each local controller could be transmitted in the background at low frequency on the CAN communication bus. This way, the full voltage amplitude of the SRB can be reached forthwith in one step. In counterpart, all local controllers are called up at each control command, even if this is unnecessary. The local controllers have to be as inexpensive and low power as possible due to the large amount used in the SRB. Therefore, the use of low power microcontrollers limits the call up frequency rate.

For direct charging of the SRB on the electrical grid, a moderate rise time is acceptable if the control frequency is sufficient. The rest of this study is therefore based on asynchronous iterative control of the local controllers performed at 20 kHz with a maximum of three slave calls per control period, hence between 1 and 12 levels for each control periods. This reduces the computing power required by the local controller sufficiently to allow the use of microcontrollers operating at frequencies as low as 48 MHz, such as the STM32F091.

3.4 Slave switches choice and thermal considerations

Switching losses are theoretically very low due to the low voltage and low switching frequency of each switch. With regard to conduction losses, the internal impedance of switches is generally proportional to their nominal voltage. The sum of the impedances of the switches in series should correspond to that of a conventional inverter. Thus, the conduction losses should be equivalent. Moreover, unlike conventional inverters, the heat distribution over the entire battery pack does not require a specific cooling system. In addition, the choice of the number of switches used in parallel makes it possible to adjust the conduction losses relative to the losses induced by the internal impedance of the cells through which the same current flows. However, there is no point in reducing the conduction losses of the switches too much, as the impedance of the cells generates large joule losses.

Thus, an impedance ratio of 1/10 has been targeted in order to make the conduction losses of the switches negligible compared to those presented by the cells themselves. From a thermal point of view, this means that the additional heating near the cells will be of the order of 10%. In other words, 90% of the heating observed in the HF SRB will be due to the self-heating of the cells. In addition to the inverter's cooling specific system saving, the prospect of carrying out cell temperature balancing offers the possibility of relieving the constraints applied on the thermal management system of the battery pack.

3.5 Master

As for the case of central units of classical BMS, the master controller centralizes all cell voltage and temperature measurements transmitted by the local controllers. It is interfaced with the outside of the HF SRB, which provides operating mode instructions (charge/discharge mode, 48 V_{DC}, 230 V_{AC}, etc...) and to which it transmits status information such as SoC, SoP and SoH battery states thanks to implemented estimators. It is also the place where all the tasks that cannot be distributed to the local controllers are carried out, such as measuring the battery pack current, managing the main power relays or monitoring their upstream and downstream voltages.

More specifically to the HF SRB management, the master controller is in charge of the optimal selection of the cells to be put in series and the others to be bypassed, as well as the transmission of the corresponding commands to the local controllers involved. The selection of the cells is performed according to a priority order provided by a balancing algorithm. This algorithm sorts the cell from multiple criteria as voltage, temperature, state of charge, of health, of power, of energy or even impedance. The master controller's computing power requirement is similar to central units of classical BMS thanks to the real time architecture described in section 4.1. A 32-bit microcontroller of around 200 DMIPS, running at frequencies up to 200 MHz such as the STM32F7 is sufficient. This kind of microcontroller is available for a target price as low as $2 for 10k units.

4 Software architecture

4.1 Real time architecture

The master controller performs asynchronous control of the remote modules to make an iterative adjustment of the overall number of active serial levels. This number is determined by a nearest level control method from a reference given by a regulation loop. The reference signal is calculated in real time in order to be able to follow sudden changes in the electrical grid voltage. Each cell is activated following an order of priority established by a balancing algorithm. This one uses cell voltage and temperature measurements as well as cell state indicators provided by the estimation algorithms. A block diagram shows interactions between those tasks in Fig. 4

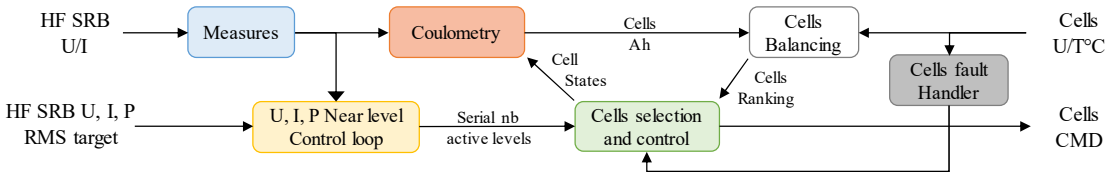


Figure 4: Block diagram of the HF SRB control algorithm performed in the master controller

It is then necessary to organise the computation of all of those tasks in order to respect the minimum control time step mentioned before. Real-time computation of the required number of active levels requires measurements of the output voltage and current, at least at the same frequency as that used for serial level control. Moreover, for cost-effective considerations, the overall HF SRB integrates only one current sensor. In our system, we choose to base the states of charge estimator on coulometry. It is then required to perform an individual coulometry estimation of each cell at the control frequency, in order to take into account the serial/bypass state of each cell. Using the same frequency to perform all those tasks simplifies the scheduling of their sequential computation.

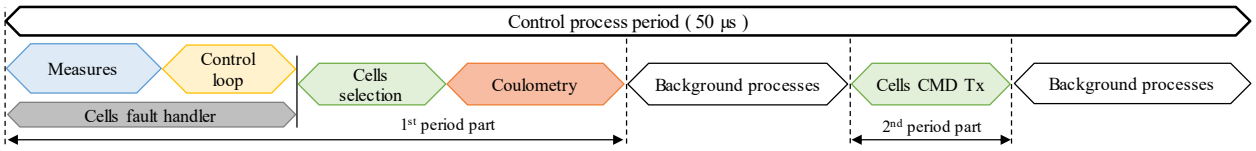


Figure 5: Schedule of a period of the HF SRB control algorithm performed in the master controller

Fig. 5 details the scheduling of those tasks gathered inside a process called “control process” and performed at each control period. One can see that most of the tasks are performed in the order of their dependencies while the balancing task is performed in background over many control periods. The control process is split into two parts. The first period part determines the command frames to send to the slaves. Its duration could have jitter due to the variability of some algorithms as cells selection and coulometry. The second part corresponds to the sending of the command frames. Both parts of the process are triggered by timer events in order to avoid jitter on the frequency of the command frame sending (see Fig. 8.c for real chronograms).

4.2 Nearest level control loop

There are two different control systems in the HF SRB’s software to manage AC voltage generation during discharge (Fig. 6) and the charge of the batteries with AC voltage (Fig. 7).

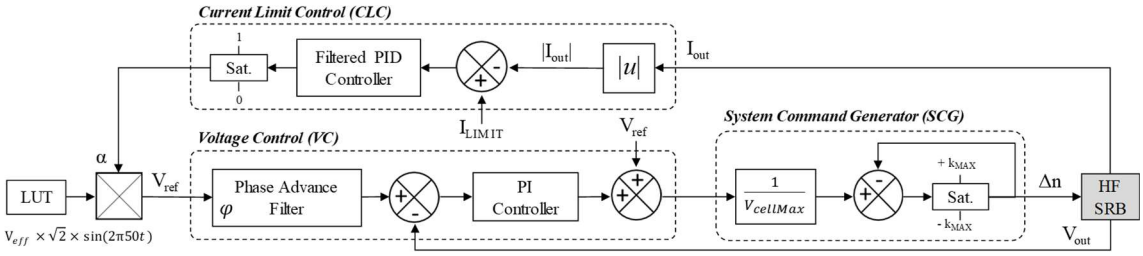


Figure 6: Synoptic bloc of the Discharge Control System

The output of each of them has a System Command Generator (SCG) bloc (Fig. 6) to convert a voltage command to the number of series cells Δn to be added or removed from the HF SRB output. k_{MAX} is the maximum number of series cells that the system can be applied at the same time (cells added if positive and cells removed if negative) and $V_{cellMax}$ is the maximum voltage of one cell (4.2V for NMC Lithium battery). The Discharge Control System (DCS) includes two sub-control loops: a Current Limit Control (CLC) to ensure that I_{out} amplitude never exceeds I_{LIMIT}, and a Voltage Control (VC) to ensure that V_{out} follows V_{ref}. The target AC voltage data points, that was obtained by sampling a 230VAC-50Hz sinusoidal signal to 20kHz, are stored in a Look-Up-Table (LUT). The latter is then multiplied by a factor α to produce V_{ref} with $0 \leq \alpha \leq 1$. α is decreased by CLC to lower V_{out} when the outputting current I_{out} is too high.

The derivative part of the Proportional-Integral-Derivative (PID) controller used in CLC has a primordial function to anticipate the variation of I_{out} when it lags behind V_{out} in the case of inductive load. As the derivative function is sensitive to the measurement noises, a Low-Pass Filter (LPF) is added to become a Filtered PID.

In VC, the Phase Advance Filter (PAF) compensates the delay φ introduced by the HF SRB system response to its command Δn. Therefore, this controller makes the control loop response faster with more stability.

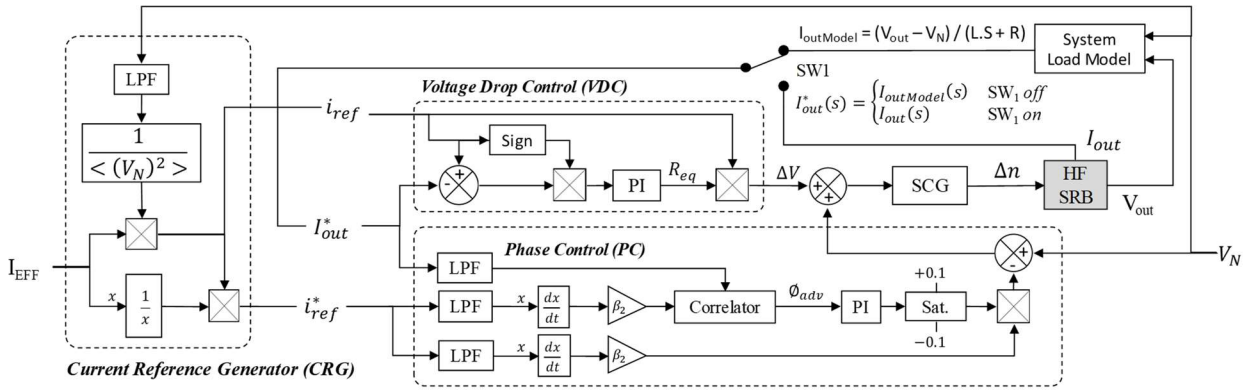


Figure 7: Synoptic Bloc of the Charge Control System

The Charge Control System (CCS) aims to charge the HF SRB from any electrical AC voltage sources by applying an output voltage V_{out} with the same pace and in phase with the charge voltage V_N, while ensuring an instantaneous charge current in phase with the both voltages V_{out} and V_N. As a result, the potential reactive power consumed by any inductive components in the system, such as L_1 and L_2, will be removed. Hence, the CCS includes three main blocs: a Current Reference Generator (CRG) bloc, a Phase Control (PC) bloc and a Voltage Drop Control (VDC) bloc. The CRG bloc generates two current references signal obtained from V_N and then, in phase with it: i_{ref} is the instantaneous current that I_{out} should look like (same pace and effective value I_{EFF}) and i^*_{ref} is the normalized value of i_{ref}. The PC bloc determines and controls the delay $\emptyset_{adv}$ of the feedback current I^*_{out} with respect to i^*_{ref} (simultaneously V_N) toward to make the charge current and voltage in phase. The LPF is a first order filter where $\tau = 100\mu s$.

Finally, the VDC bloc controls the differential voltage ΔV between V_N and V_{out} to keep I^*_{out} close to i_{ref}. To obtain ΔV, the control loop estimates the equivalent resistor R_{eq} between batteries and the AC charger that includes batteries ESR, inductors internal resistance, wire resistance and so on. In practice, V_N is not directly connected to V_{out} at the start-up of the control system to avoid short-circuiting and damaging the charger and the HF SRB system. The solution is to synchronize V_N and V_{out} when $I_{out} = 0A$ (SW_1 off) and to make V_N's amplitude slightly higher than V_{out}'s one to allow current flows from AC charger to HF SRB after switching on SW_1. To do this, I^*_{out} is first equal to the modelled current $I_{outModel}$ until $|\emptyset_{adv}| < 0.01$, the necessary condition to switch on the power relay SW_1, and then use I_{out} as a feedback input current.

5 Experimental results

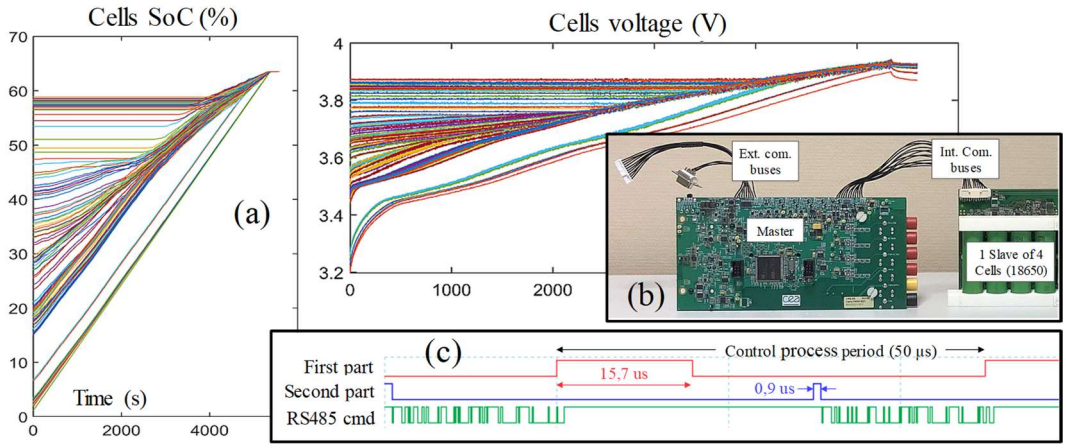


Figure 8: Cells balancing of HF SRB on direct charge with electrical grid and control process period

Following experimentations are performed on a real HF SRB of 1 master and 32 slaves integrating 128 NMC cells for a rated power output of 2 kW. An overall capacity of 1 kWh is achieved in a volume of 14.5 L. The Master and one Slave unit are shown in Fig. 8.b and a chronogram of the control process period is shown in (c).

5.1 Cells balancing

A complete charge performed at C/2 on the electrical grid from an initial SoC imbalance of 60% shows that the 128 cells are perfectly balanced before the end of charge. The SoC and cell voltage signals transmitted from CAN bus are reported on Fig. 8.a.

5.2 Waveform generation

Fig. 9 shows the experimental waveforms when a battery of 128 VTC6 cells was discharging (a) and when it was charged up at the rated power of 280 W (b). THD measurements has been performed from a HIOKI PW6001-16 used with a current probe HIOKI 20A CT 6841-05. Those are reported as superposed screen captures in Fig. 9. The difference of current displayed on the HIOKI screen capture is due to the use of 5 wire turns around the current probe to improve its precision.

One can see that the voltage THD of the HF SRB output is less than 0.3% when it discharges with a serial inductance of 100 µH. For security reason, a rectifier diode stage has been added at the charging input of the HF SRB to prevent outputting current on its connector. Indeed, a male plug is used in order to demonstrate the simplicity of connecting the prototype to the electrical grid. The control loop has been modified to follow the incoming rectified voltage while absorbing a near sinusoidal charging current waveform and in phase with this voltage. The current THD was about 15.6% with a serial inductance of 1.1 mH and a charge current of only 1.2 A_{RMS}. A better current THD should be achieved for higher charge current if more than one parallel cell is used.

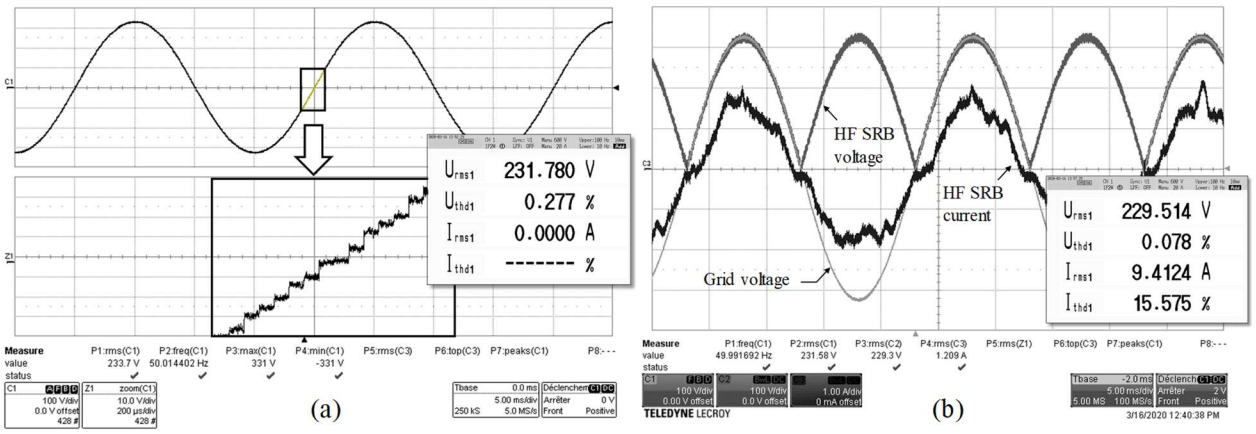


Figure 9: HF SRB 230Vac 50Hz waveforms

5.3 Efficiency

The efficiency is measured in discharge mode and at different current levels on one slave of 4 NMC cells and is extrapolated to estimate the efficiency of the full HF SRB. The slave is driven to generate a sinusoidal voltage of +/- 4 serial levels at 50 Hz. The applied discharge powers vary from 3 W_{RMS} to 125 W_{RMS} using an adjustable power resistor from 100 to 0 Ω. The equipment used to perform the efficiency measurement is a HIOKI PW6001-16. Each of the 4 cells is instrumented with a current probe HIOKI 20A CT 6841-05 +/- 0.3% and their voltage is measured directly by the measuring device at +/- 0.02%. The output current of the slave is instrumented with a HIOKI 50A probe +/- 0.05% and its voltage is measured directly by the measuring instrument.

The power losses are depicted on Fig. 10. One can see that the losses curve has a typical quadratic growth pattern. The substantially constant power losses for the lowest powers indicates the static consumption of the slave. This consumption is about 580 mW per slave and includes the power supply of the local control circuits, the cells voltages and temperatures measurement circuits, the cells serial and bypass switches gate drivers as well as the H-bridge switches gate drivers.

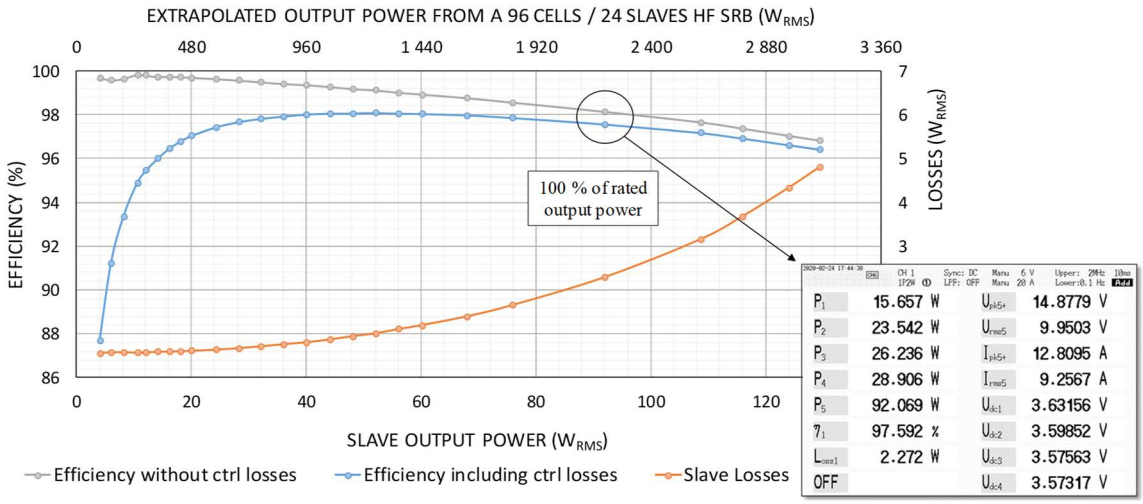


Figure 10: Slave HF SRB discharge efficiency over 50Hz staircase shape sine waveform

As shown on Fig. 10, for an output power of 92.069 W_{RMS}, the switching current flowing through the switches is 9.2567 A_{RMS} and power losses are 2.272 W_{RMS}. Knowing the losses offset of 580 mW and that switching losses can be neglected; the conductive losses should be around 1.692 W_{RMS}. At each time, the number of serial switches through which the serial current flows is composed as follows: one for each cell and two for the full H-bridge. Each switch uses the same reference which have a Ron of 1 mΩ (PSMN0R9-25YLC). Thus, the conducting power losses from those MOSFET should be around 514 mW_{RMS} which is around a third of the amount of measured losses. This tends to show that the total impedance of the conducting tracks is of the same order than the "on" state switch impedances. Therefore, the power losses are well distributed between the switches and power tracks, which allows a good distribution of the heat release over the entire PCB of the local controller. Moreover, those power losses may represent less than 10% of the overall battery loss as the impedance of the cells is more than ten times higher. All this shows that there is no need of a specific cooling for the HF SRB.

Efficiency curve of one slave is also depicted on Fig. 10. To extrapolate the efficiency of the HF SRB charging over the electrical network, we multiply the powers on x-axis by the number of slaves required to generate a sine waveform of 230 V_{RMS} (hence a factor of 24 for cells at rated voltage of 3.6 V). The efficiency of the HF SRB is also depicted with subtracting the consumption of the control electronics (24 times 580 mW) as it is usual in efficiency measurements carried out on power converters. It can be seen that the efficiency of the HF SRB is above 98% up to 2300 W_{RMS} of power delivery, which corresponds to a discharge rate of 4.5 C. These results are among the best of the state of the art [21].

6 Conclusion

The feasibility of a microcontroller based Self-Reconfigurable Battery able to charge itself directly on the electrical grid has been demonstrated. This has been possible thanks to the use of a Near Level Control with iterative commands. The system distribution in Master and Slaves modules has allowed to reduce the complexity of the switch management by adding an abstraction layer. This leads to implement a total number of 128 serial levels, although a greater number of levels is possible. The real-time management of cell switches allows a faulty cell to be replace at any time without disturbing the generated output voltage. The measurements made on the

demonstrator show very good results in term of efficiency (up to 98% including control consumption) and output voltage THD.

References

[1] L. Lu, X. Han, J. Li, J. Hua, and M. Ouyang., *A review on the key issues for lithium-ion battery management in electric vehicles*, Journal of Power Sources, ISSN 0378-7753, 226(2013), 272-288

[2] W.F. Bentley, *Cell balancing considerations for lithium-ion battery systems*, IEEE (Proceedings of the Annual Battery Conference on Applications and Advances), ISSN 1089-8182, 1997, 223-226

[3] T. Baumhöfer, M. Brühl, S. Rothgang, and D. U. Sauer, *Production caused variation in capacity aging trend and correlation to initial cell performance,* Journal of power sources, ISSN 0378-7753, 247(2014), 332-338

[4] D. Andrea, *Battery Management Systems for large Lithium-Ion battery packs,* ISBN 1608071049, Artech House, 2010

[5] S. Ci, N. Lin, and D. Wu, *Reconfigurable Battery Techniques and Systems: A Survey,* IEEE Access, ISSN 21693536, 4(2016), 1175-1189

[6] L. He, L. Gu, L. Kong, Y. Gu, C. Liu, and T. He, *Exploring Adaptive Reconfiguration to Optimize Energy Efficiency in Large-Scale Battery Systems*, ISSN 10528725, IEEE Real-Time systems, 2013, 118-127

[7] A. Davis, Z. M. Salameh, and S. S. Eaves, *Evaluation of lithium-ion synergetic battery pack as battery charger*, IEEE Transactions on Energy Conversion, ISSN 08858969, 14(1999), 830-835

[8] A. Davis, Z. M. Salameh, and S. S. Eaves, *Comparison of a synergetic battery pack drive system to a pulse width modulated AC induction motor drive for an electric vehicle,* IEEE Trans. Energy Conv., 14(1999), 245-250

[9] A. Genovese, F. Ortenzi, C. Villante, *On the energy efficiency of quick DC vehicle battery charging*, presented at EVS28 and published in World Electric Vehicle Journal, ISSN 20326653, 7(2015), 540-576

[10] Z. Zheng, K. Wand, L. Xu, and Y. Li, *A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles*, IEEE Transactions on Power Electronics, ISSN 08858993, 29(2014), 3537-3546

[11] S. D'Arco, M. Quraan, P. Tricoli, and L. Piegari, *Low frequency operation of Modular Multilevel Converters with embedded battery cells for traction drives*, SPEEDAM, ISBN 978-1-5090-2067-6, 2016, 1375-1382

[12] D. D. Simone and L. Piegari, *Integration of stationary batteries for fast charge EV charging stations*, Energies, ISSN 19961073, 12(2019)

[13] H. Akagi, and L. Maharjan, *A battery energy storage system based on a multilevel cascade PWM converter*, IEEE, ISSN 2165-0454, 2009, 9-18

[14] M. Quraan, T. Yeo, and P. Tricoli, *Design and Control of Modular Multilevel Converters for Battery Electric Vehicles*, IEEE Transactions on Power Electronics, ISSN 0885-8993, 31(2016), 507-517

[15] F. Gao, X. Gu, Z. Ma, C. Zhang, *Redistributed Pulsewidth Modulation of MMC Battery Energy Storage System under Submodule Fault Condition*, IEEE Trans. on Power Electron., ISSN 0885-8993, (35)2020, 2284-2294

[16] D. D. Simone, L. Piegari, and S. D'Arco, *Comparative Analysis of Modulation Techniques for Modular Multilevel Converters in Traction Drives*, SPEEDAM, ISBN 978-153864941-1, 2018, 593-600

[17] D. Kraus, E. Specht, T. Merz, M. Hiller, *Optimized Real-Time Control for Modular Multilevel Converters using Adaptive Neural Networks*, EPE'19 ECCE, ISBN 978-9-0758-1531-3, 2019

[18] H. Kim and K. G. Shin, *On Dynamic Reconfiguration of A Large-Scale Battery System*, IEEE Real-Time and Embedded Technology and Applications Symposium, ISSN 1545-3421, 2009, 87-96

[19] H. Kim and K. G. Shin, *DESA: Dependable, efficient, scalable architecture for management of large-scale batteries*, IEEE Transactions on Industrial Informatics, ISSN 1551-3203, 8(2012), 406-417

[20] T. Morstyn et. Al., *Distributed Control for State-of-Charge Balancing Between the Modules of a Reconfigurable Battery Energy Storage System*, IEEE Transactions on Power Electronics, ISSN 0885-8993, 31(2016), 7986-7995

[21] Z. Gao, Q. Lu, *A Hybrid Cascaded Multilevel Converter Based on Three-Level Cells for Battery Energy Management Applied in Electric Vehicles*, IEEE Trans. Power Electron., ISSN 0885-893, 34(2019), 7326-7349

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